SC13154HP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	:	Group Art Unit: 2822
Hei Ming SHIU et al.	:	Examiner: Thanh Y. Tran
Serial No.: 10/807,527	:	Confirmation No.: 3435
Filed: March 24, 2004	:	Attorney Docket No.: **SC13154HP**
For: **LAND GRID ARRAY PACKAGED DEVICE AND METHOD OF FORMING SAME**	:	

Article I. Certificate of Submission

I hereby certify that this correspondence is being submitted to the U.S.P.T.O., Alexandria, VA.

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Nov. 6, 2006
Date of Submission

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Charles Bergere
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ON APPEAL FROM THE PRIMARY EXAMINER
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELANTS' BRIEF UNDER 37 C.F.R. §41.37

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I. REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., which has its headquarters in Austin, Texas.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any other appeals, interferences or judicial proceedings that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-6 and 8-20 are active in the present application. Claim 7 has been cancelled.

Claims 1-6 and 8-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 2004/0097081 (Igarashi) in view of U.S. Patent No. 5,568,363 (Kitahara).

The rejection of claims 1-6 and 8-20 is being appealed.

IV. STATUS OF AMENDMENTS

A final rejection was mailed on June 7, 2006. An Argument with an amendment (grammatical correction) to claim 10 was filed on August 7, 2006. An Advisory Action was mailed on September 8, 2006 stating that the Amendment did not place the application in condition for allowance. Thus, the amendment to claim 10 is presented again herein.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a method of packaging an integrated circuit die without the use of a lead frame. Instead, a foil sheet is provided and a layer of solder is applied to a surface of the foil sheet. The die is then attached to the foil sheet by way of the solder layer. Die bonding pads are connected to the solder layer with wires by wirebonding. The die and wires are encapsulated with a mold compound and then the foil sheet is separated from the die and the wires. A portion of the solder remains on the bottom of the die and the tips of the wires. It should be noted that the foil sheet is not a part of the final packaged device.

Independent claim 1 recites a method of packaging an integrated circuit die 12 (FIG. 2A). The die 12 may be any type of circuit, such as a digital signal processor (see paragraph **[0022]**, lines 1-4).

A foil sheet 30 is provided (see FIGS. 2A-2D). The foil sheet 30 comprises a relatively flat, bare sheet of metal, such as copper or aluminum (para. **[0023]**, lines 5-6). A single layer of solder 32 is formed on one side of the foil sheet 30, such as by screen printing a layer of high temperature solder paste on the foil sheet (para. **[0023]**, page 6, lines 1-9).

The die 12 is attached to the solder layer on the foil sheet. The die 12 includes a layer of metal 34 on a bottom

side thereof to facilitate attachment to the solder layer 32. (para. **[0024]**, lines 7-9).

Next, bonding pads 14 on the die 12 are electrically connected to the solder layer 32 with wires 16, such as by using a ball bonding process in which a heated tip of wire is pressed into the solder 32, forming a squashed ball 38 (see FIG. 2B and para. **[0026]**).

After the wires are connected between the die bonding pads and the solder, the die and the electrical connections are encapsulated with a mold compound 20 (see FIG. 2C and para. **[0027]**).

Finally, the foil sheet 32 and a portion of the solder layer 32 are separated from the encapsulated die 12 and wires 16, such as by a reflow process (see FIG. 2D and para. **[0028]**).

Independent claim 15 is similar to claim 1 except that it is directed to simultaneously forming a plurality of integrated circuit packages. (See FIGS. 2A-2E).

Independent claim 18 uses the method recited in claim 1 to form a multi-chip module. That is, at least two integrated circuit dies are attached to the foil sheet with some of the bonding pads on the two dies being connected to the solder layer with wires and some of the bonding pads of the two dies being connected to each other with wires. Both dies and the wires are encapsulated and then the foil sheet is removed, thus forming the multi-chip module. (See FIG. 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1-6 and 8-20 unpatentable pursuant to 35 U.S.C. § 103(a) over U.S. 2004/0097081 (Igarashi) in view of U.S. Patent No. 5,568,363 (Kitahara)?

VII. ARGUMENT

1. Independent Claim 1

Independent claim 1 stands rejected under 35 U.S.C. § 103 as unpatentable over Igarashi in view of Kitahara.

Igarashi, like the present invention, teaches a method of packaging a semiconductor IC. Although the final package (Igarashi FIG. 14) looks somewhat similar to the final package (FIG. 2E) of the present invention, the respective packages are actually quite different, and thus, the methods for making these two packages also are different.

Igarashi forms a laminated plate 10 using first, second and third conductive films 11, 12 and 13. A fourth conductive film 14 also is adhered to the plate 10. An etching process is performed to form pads 14A (Igarashi at [0068]). Additional complex and expensive etching steps are performed to remove portions of the films 11 and 13 (Igarashi at [0072] to [0079] and FIGS. 1-8).

Igarashi attaches the die 19 to the laminated plate 10. Wires are then attached from die bond pads to built up pads 14A. (See Igarashi FIG. 9).

Igarashi FIG. 10 illustrates an encapsulation step. After encapsulation, one of the conductive films (i.e., the second conductive film (12)) of the laminated plate 10 is

removed (see FIG. 11). Then, an additional resin layer 23 is coated onto the bottom of the package and finally, electrodes 24 are formed by screen printing a solder cream onto the bottom of the package and performing a reflow.

Kitahara is directed to a lead frame type packaged device. Kitahara is cited for teaching in FIGS. 1-2 a bare metal sheet 3 (See first Office Action at page 3, lines 12-17) and that this bare metal sheet 3 could replace the laminated plate 10 of Igarashi. This logic was reiterated in the Final Office Action at page 8, lines 15-20 and the Advisory Action at page 2.

Applicants had previously argued the metal sheet 3 of Kitahara is different from the metal sheet of the present invention because, *inter alia*, the metal sheet of the present invention is removed and does not form a part of the final package, whereas in Kitahara, the metal sheet is an integral part of the final package. That is, the metal sheet forms bendable leads. Similarly, in Igarashi, the laminated plate 10 is an integral part of the final packaged device.

The Examiner disagreed with the above-argument, stating that the limitation of the foil sheet being removed is not a claim limitation. Applicants respectfully disagree.

Claim 1 recites in the last step, "separating the foil sheet from the die and the plurality of wires, thereby forming the packaged integrated circuit." Thus, the fact

that the foil sheet is not a part of the final package is explicitly recited in the claims.

Referring again to Igarshi, the rejection avers that Igarashi discloses all of the claimed steps except for the bare metal sheet, and that a bare metal sheet is disclosed by Kitahara. See, Final Rejection mailed June 7, 2006, page 8, lines 13-15.

As mentioned above, Igarashi is directed to a method of packaging a semiconductor IC. However, instead of using a single layer of solder to form the package terminals, Igarashi teaches building the package with a patterned, multi-layer conductive laminate (*i.e.*, the laminated plate 10).

Igarashi forms the laminated plate 10 using first, second and third conductive films 11, 12 and 13. See Igarashi para. [0060]. A fourth conductive film 14 also is adhered to the plate 10. An etching process is performed to form pads 14A (Igarashi at [0068]). Additional complex and expensive etching steps are performed to remove portions of the films 11 and 13 (Igarashi at [0072] to [0079]).

In contrast, the present invention uses a single foil sheet with a layer of solder.

Igarashi FIG. 1 shows the formation of the multi-layer laminate. Compare to FIG. 2A of the present application, which shows a foil sheet and a single layer of solder.

Igarashi FIGS. 2-8 show the complex steps required to prepare the multi-layer laminate prior to attaching the IC die. The present invention does not require these complex processing steps.

Igarashi FIG. 9 shows an IC die attached to the multi-layered laminate, and bond wires attached to the multi-layered laminate. Compare Igarashi FIG. 9 to FIG. 2A of the present application, it can be seen that Igarashi teaches a multi-layered laminate (11A, 12, 13, 14A) and the present invention uses only a single layer of solder 32 formed on a foil sheet 30. So, not only is the IC attached to a multi-layered laminate 10, but the bond wires 20 are attached to the multi-layered laminate 10. In the present invention, the bond wires 16 are attached directly to the single solder layer.

Igarashi FIG. 10 shows the die being encapsulated; which corresponds to FIG. 2C of the present application.

Igarashi FIG. 11 shows one of the conductive films 12 used to form the laminated plate 10 being removed; FIG. 2D of the present application, shows the foil sheet 30 and solder layer 32 being removed. Note that in the present application, the ball bonds are now exposed, whereas in Igarashi, the ball bonds are not exposed; rather the ball bonds are separated from the outside of the package by the layers 13, 11A and 14.

Igarashi FIG. 13 shows the steps of screen printing with solder cream and then reflow. In contrast, the present invention does not require such an additional step

of screen printing solder cream because the package is formed using a layer of solder (32).

Finally, compare Igarashi FIG. 14 with FIG. 2E of the present application. Igarashi's final package has electrodes 24 that are connected to the IC bond pads by way of the conductive layers 13, 11A and 14. FIG. 2E of the present application illustrates that the ball bonds of the bond wires 16 form the package terminals and there is no plate or metal sheet located between the package terminals and the die bond pads.

As previously discussed, the Office Action recognizes that the present invention uses a foil sheet with a solder layer thereon as opposed to the complex, multi-layered structure taught by Igarashi, so Kitahara is cited as disclosing the use of a bare metal sheet.

The metal sheet (3) of Kitahara is a typical lead frame. A bumped die is attached to the lead frame. More particularly, bumps (11) are attached to leads (3) and then covered with a sealing resin (2). Kitahara differs from the present invention in that the present invention does not involve a lead frame or metal leads. Note that the leads (3) of Kitahara form an important part of the final package; whereas in the present invention, the foil sheet does not form any part of the final package. Rather, the "leads" of the present invention are the squashed ball bonds formed by the wire bonding and reflow processes. Kitahara does not use any wire bonding processes, nor form any ball bonds.

Furthermore, the copper sheet of Kitahara cannot be properly combined with the process taught by Igarashi because Kitahara is a lead frame type process, so attaching the wires (20) of Igarashi to the leads (3) of Kitahara would not form the ball bonds that act as terminals of the present invention.

More particularly, if the lead frame of Kitahara were substituted for the substrate (11, 13, 14) of Igarashi, one would have the wires extending from the IC bond pads to the leads of the Kitahara lead frame, and then solder balls would have to be attached to the bottom of the leads to form the terminals. Note that the lead frame then would not be removable in the same manner that the sheet is removed in the present invention. Thus, the Kitahara lead frame is not removable and would require the attachment of solder balls to form contacts akin to the terminals of the present invention. As the present invention does not include such steps, the method of the present invention differs from a method taught by a combination of Igarashi and Kitahara.

As discussed above and defined in independent claims 1, 15 and 18, the present invention uses a foil sheet with a single layer of solder. The package terminals are formed by ball bonding to the solder layer, performing a reflow, and then removing the foil sheet. The final package includes neither a lead frame nor a multi-layer laminated plate. The present invention is therefore very different from the processes taught by Igarashi and Kitahara, either alone or in combination. Accordingly, Applicants

respectfully request that the rejection under section 103 be withdrawn.

Each of the independent claims 1, 15 and 18 of the present invention recites the use of a foil sheet with a single layer of solder. The package terminals are formed by ball bonding to the solder layer, performing a reflow, and then removing the foil sheet. There is neither a lead frame nor a multi-layer laminated plate used in the process. The present invention is therefore very different from the processes taught by Igarashi and Kitahara, either alone or in combination. Accordingly, Applicants respectfully request that the rejection under section 103 be withdrawn.

It is well settled that in order to establish a prima facie case of obviousness with respect to a claim, at least two criteria must be met: (1) the prior art references must suggest to one of ordinary skill in the art to make the subject matter defined by the claims in issue and (2) the prior art references must provide one of ordinary skill in the art with a reasonable expectation of success in so making the subject matter defined by the claims in issue. Both the suggestion and the reasonable expectation must be found in the prior art references, not in the disclosure of the patent application in issue. See, *e.g.*, *In re Vaeck*, 947 F.2d 488, 493, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

Appellants submit that one of skill in the art would not look to Kitahara to learn how to form a packaged device without using a lead frame. Moreover, neither reference

provides a suggestion of forming a packaged device that does not include a lead frame or carrier as part of the final package. Since no suggestion of this feature is provided, no reasonable expectation of success is provided by the combination of references. No *prima facie* case of obviousness has been established and so the rejection is improper and should be reversed. Appellants therefore request the reversal of the rejection of claims 1, 15 and 18 under 35 U.S.C. 103.

2. Claims 2-6 and 8-20

For at least the same reasons that claim 1 is patentable over Igarashi and Kitahara, claims 15, 18 and the dependent claims are patentable.

For at least the reasons set forth above, Appellants respectfully submit that the claims of the present application are allowable over the art cited during prosecution and respectfully request that the rejection of claims 1-6 and 8-20 be withdrawn.

Respectfully submitted,

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Nov. 6, 2006
(Date)

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CLAIMS APPENDIX

1. (previously presented) A method of packaging an integrated circuit die, comprising the steps of:

providing a foil sheet;

forming a single layer of solder on a first side of the foil sheet;

attaching a first side of an integrated circuit die to the single solder layer on the foil sheet, wherein the first side of the die includes a layer of metal thereon and a second, opposing side of the die includes a plurality of bonding pads;

electrically connecting the bonding pads to the single solder layer on the foil sheet with a plurality of wires;

encapsulating the die, the electrical connections, and the first side of the foil sheet with a mold compound; and

separating the foil sheet from the die and the plurality of wires, thereby forming a packaged integrated circuit.

2. (original) The method of packaging an integrated circuit according to claim 1, wherein the foil sheet comprises a bare metal sheet.

3. (original) The method of packaging an integrated circuit according to claim 2, wherein the metal sheet comprises one of copper and aluminum.

4. (original) The method of packaging an integrated circuit according to claim 1, wherein the solder is formed on the foil sheet via a screen printing process.

5. (original) The method of packaging an integrated circuit according to claim 4, wherein the solder layer has a thickness of about 0.1 mm.

6. (previously presented) The method of packaging an integrated circuit according to claim 1, further comprising performing a first reflow process after the die attach step, wherein the first reflow process melts the solder, thereby securing the die to the foil sheet.

7. CANCELLED

8. (original) The method of packaging an integrated circuit according to claim 1, wherein the plurality of wires are attached to the bonding pads and the solder via a wire bonding process.

9. (original) The method of packaging an integrated circuit according to claim 1, wherein the wirebonding process comprises a ball bonding process.

10. (previously presented) The method of packaging an integrated circuit according to claim 9, wherein the ball bonding process forms squashed ball bonds having a diameter of about 0.25 mm are formed on the foil sheet, wherein said ball bonds function as package terminals.

11. (original) The method of packaging an integrated circuit according to claim 1, wherein the wires have a diameter of about 50 um to about 100 um.

12. (original) The method of packaging an integrated circuit according to claim 1, wherein the foil sheet is separated from the die and the wires via a second reflow process.

13. (previously presented) The method of packaging an integrated circuit according to claim 12, wherein a portion of the solder remains attached to the wires and the die after the foil sheet is separated therefrom.

14. (original) The method of packaging an integrated circuit according to claim 1, wherein the more than one die is attached to the foil sheet, and after the foil sheet is separated from the die and the wires, the die and the wires connected to the respective die are separated from each other such that multiple packaged devices are formed substantially simultaneously.

15. (previously presented) A method of forming a plurality of integrated circuit packages, comprising the steps of:

providing a sheet of metal foil;

forming a layer of high temperature solder on a first side of the foil sheet via a screen printing process;

attaching first sides of a plurality of integrated circuit dies to the single solder layer on the foil sheet, wherein the first side of each of the die includes a layer of metal thereon and a second, opposing side of each of the die includes a plurality of bonding pads;

performing a first reflow process for securing the plurality of integrated circuit dies to the metal foil;

electrically connecting the bonding pads to the single solder layer on the foil sheet with a plurality of wires

via a wirebonding process, wherein first ends of the wires are attached to the bonding pads and second ends of the wires are attached to the foil sheet;

encapsulating the integrated circuit dies, the electrical connections, and the first side of the foil sheet with a mold compound;

separating the foil sheet and the solder layer from the integrated circuit dies, second ends of the plurality of wires, and the mold compound via a second reflow process, wherein only a portion of the solder layer is removed from the dies and the second ends of the plurality of wires; and

separating the encapsulated integrated circuit dies and the wires connected thereto from other ones of the encapsulated integrated circuit dies, thereby forming a plurality of packaged integrated circuits.

16. (previously presented) The method of packaging an integrated circuit according to claim 15, wherein squashed ball bonds having a diameter of about 0.25 mm are formed on the foil sheet, wherein said ball bonds function as package terminals.

17. (original) The method of forming a plurality of integrated circuit packages of claim 15, wherein the separating step comprises the step of saw singulating the encapsulated die from adjacent encapsulated dies.

18. (previously presented) A method of forming a multi-chip module, comprising the steps of:

providing a sheet of metal foil;

forming a single layer of high temperature solder on a first side of the foil sheet via a screen printing process;

attaching first sides of at least two integrated circuit dies to the single solder layer on the foil sheet, wherein the first side of each of the die includes a layer of metal thereon and a second, opposing side of each of the die includes a plurality of bonding pads;

performing a first reflow process for securing the at least two integrated circuit dies to the metal foil;

electrically connecting a first portion of the bonding pads of each of the at least two dies to the single solder layer on the foil sheet with a plurality of first wires via a first wirebonding process, wherein first ends of the first wires are attached to the bonding pads and second ends of the first wires are attached to the foil sheet;

electrically connecting the at least two dies to each other by connecting a second portion of the bonding pads of a first one of the die to a second portion of the bonding pads of a second one of the dies with a plurality of second wires via a second wirebonding process;

encapsulating the at least two integrated circuit dies, the electrical connections, and the first side of the foil sheet with a mold compound; and

separating the foil sheet and the solder layer from the at least two integrated circuit dies, second ends of the plurality of first wires, and the mold compound via a second reflow process, wherein only a portion of the solder layer is removed from the at least two dies and the second ends of the plurality of wires.

19. (original) The method of forming a multi-chip module of claim 18, further comprising the steps of:

saw singulating the encapsulated die from adjacent encapsulated dice.

20. (original) The method of forming a multi-chip module of claim 18, further comprising the steps of:

attaching a passive device to the solder on the foil sheet; and

electrically connecting the passive device to at least one of the at least two dies, and wherein the passive device is encapsulated with the mold compound.

EVIDENCE APPENDIX UNDER 37 CFR 41.37(c)(1)(ix)

There is no evidence that has been entered into the record by the Examiner that is relied upon in this appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.